REMARKS

Reconsideration and allowance of the present application are respectfully requested. Claims 1-9 remain pending in the application. By this Amendment claim 1 is amended.

In numbered paragraph 2 of the Office Action, independent claim 1, along with various dependent claims, is rejected as being unpatentable over U.S. Patent 6,609,167 (Bastiani et al.) in view of U.S. Patent 6,718,413 (Wilson et al.) and US 2003/0051077 (Fengler). In numbered paragraph 3, page 6 of the Office Action, dependent claim 9 is rejected as being unpatentable over the Bastiani et al. patent, in view of the Wilson et al. patent and the Fengler publication, and further in view of.U.S. Patent 5,555,430 (Gephardt et al.). These rejections are respectfully traversed.

Applicants have disclosed a transceiver configured for use with a multi-tier system bus that allows for the flow of information to be managed among plural processors by connecting processors within modules on a local bus, which is then connected to the system bus by way of a gateway (e.g., paragraph [0014]). As exemplified in Fig. 2, a transmitter portion provides buffering and interleaved output of direct memory access and control actions packet types. A receiver portion provides input discrimination and individual buffering of direct memory access and interrupt control actions packets along with specialized control functions, e.g., reset, timer, broadcast, etc. (abstract).

Applicants have disclosed that two basic types of operations are supported, including DMA operations and control operations (e.g., paragraph [0093]). As exemplified in Fig. 1, a system controller 104 can control and arbitrate access to the

system bus 102 (paragraph [0013]). For example, control action packets can preempt a DMA packet to be transferred (e.g., paragraph [0096]).

The foregoing features are broadly encompassed by claim 1, which recites a transceiver for use within a multi-tier system bus configuration, including, among other features, means for buffering instructions received via the system bus to provide a separate buffering of control actions from DMA operations; wherein access to the multi-tier system bus is arbitrated such that control actions preempt DMA operations.

The Bastiani et al. patent discloses a packet generator/decoder 358 that sends and receives data packets to and from a connected device. As shown in Fig. 41, the packet generator/decoder is common for both send and receive, and does not discriminate between types of input for separate buffering. The Bastiani et al. patent would not have taught or suggested a transceiver for use within a multi-tier system bus configuration possessing the structural features for buffering instructions received via a system bus to provide a separate buffering of control actions from DMA operations, as recited in claim 1. Further, the Bastiani et al. relates to individual Tx/Rx connections to respective devices, but would not have taught or suggested connections to a system bus, wherein access to the multi-tier system bus is arbitrated such that control actions preempt DMA operations, as recited in claim 1.

The Wilson et al. patent does not cure the deficiencies of the Bastiani et al. patent. The Wilson et al. patent relates to a host adapter coupled to one or more I/O devices arbitrating for the bus (abstract). The Wilson et al. patent discloses a plurality of devices in contention for a bus for data transfer to a host adapter (col. 4, lines 3-7). An interrupt asserted to the processor indicates that a device has

transferred data (col. 4, lines 7-12). However, the Wilson et al. patent would not have taught or suggested specifically the structural features for buffering instructions received via a system bus to provide a separate buffering of control actions from DMA operations, as recited in claim 1. Further, the Wilson et al. disclosure is not specific to an arbitration involving preemption of DMA operations, as recited in claim 1.

The Fengler publication does not cure the deficiencies of the Bastiani et al. patent and the Wilson et al. patent. As shown in Fig. 2, the Fengler publication discloses a peripheral device 102 comprising components connected to a local interface 214. The processing device 200 is adapted to execute commands stored in memory 202 to coordinate the overall operation of the peripheral device 102 (paragraph [0020]). However, the Fengler publication would not have taught or suggested specifically the structural features for buffering instructions received via a system bus to provide a separate buffering of control actions from DMA operations, as recited in claim 1. Further, the Fengler disclosure is not specific to an arbitration involving preemption of DMA operations, as recited in claim 1.

The Gephardt et al. patent does not cure the deficiencies of the Bastiani et al. patent, the Wilson et al. patent, and the Fengler publication. The Gephardt et al. patent was applied for its disclosure of interrupt management in a multiprocessing system (col. 22, line 61 through col. 23, line 17). However, the Gephardt et al. patent would not have taught or suggested specifically the structural features for buffering instructions received via a system bus to provide a separate buffering of control actions from DMA operations, as recited in claim 1. Further, the Gephardt et

al. disclosure is not specific to an arbitration involving preemption of DMA operations, as recited in claim 1.

For the foregoing reasons, Applicant's claim 1 is allowable. The remaining claims depend from independent claim 1 and recite additional advantageous features which further distinguish over the documents relied upon by the Examiner. As such, the present application is in condition for allowance.

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the application is in condition for allowance and a Notice of Allowance is respectfully solicited.

Respectfully submitted,

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